AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a high-threshold N-channel type MIS field effect transistor connected between a real high-potential power supply line and a pseudo high-potential power supply line; ~~and~~

a load circuit having a low-threshold P-channel type MIS field effect transistor and a low-threshold N-channel type MIS field effect transistor; and

a waveshaping circuit which receives a control signal for controlling said high-threshold N-channel type MIS field effect transistor, and performs waveshaping so that an output signal of said waveshaping circuit rises slower than said control signal, wherein:

a first power supply terminal of said load circuit is connected to said pseudo high-potential power supply line, and a second power supply terminal of said load circuit is connected to a real low-potential power supply line; ~~and~~

a back gate of said low-threshold P-channel type MIS field effect transistor is connected to said pseudo high-potential power supply line, and a back gate of said low-threshold N-channel type MIS field effect transistor is connected to said real low-potential power supply line;

said output signal of said waveshaping circuit is supplied to a gate of said high-threshold N-channel type MIS field effect transistor; and

said waveshaping circuit comprises a high-threshold final-stage MIS field effect transistor, or a plurality of high-threshold final-stage MIS field effect transistors connected in series.

Claims 2 and 3. (Cancelled)

4. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 1 [[3]], wherein said high-threshold N-channel type MIS field effect transistor is configured as a source follower, and a voltage on said pseudo high-potential power supply line connected to the source of said high-threshold N-channel type MIS field effect transistor rises in response to the output signal of said waveshaping circuit supplied to said gate.

5. (Cancelled)

6. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 1 [[3]], wherein said waveshaping circuit comprises a digital/analog converter.

7. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 6, wherein said load circuit comprises a memory circuit, and said digital/analog converter outputs a voltage that is lower than an operating voltage of said

memory and that only guarantees the retention of stored contents, thereby achieving a reduction in backup standby power consumption.

8. (Currently Amended) A semiconductor integrated circuit device comprising:

a high-threshold N-channel type MIS field effect transistor connected between a real high-potential power supply line and a pseudo high-potential power supply line, said high-threshold N-channel type MIS field effect transistor being controlled by receiving a rising control signal to a gate thereof; ~~and~~

a load circuit having a low-threshold P-channel type MIS field effect transistor and a low-threshold N-channel type MIS field effect transistor; and

a waveshaping circuit which receives a control signal for controlling said high-threshold N-channel type MIS field effect transistor, and performs waveshaping so that an output signal of said waveshaping circuit rises slower than said control signal, wherein:

a first power supply terminal of said load circuit is connected to said pseudo high-potential power supply line, and a second power supply terminal of said load circuit is connected to a real low-potential power supply line; ~~and~~

a back gate of said low-threshold P-channel type MIS field effect transistor is connected to said pseudo high-potential power supply line, and a back gate of said low-threshold N-channel type MIS field effect transistor is connected to said real low-potential power supply line;

said output signal of said waveshaping circuit is supplied to a gate of said high-threshold N-channel type MIS field effect transistor; and

said waveshaping circuit comprises a high-threshold final-stage MIS field effect transistor, or a plurality of high-threshold final-stage MIS field effect transistors connected in series.

9. (Currently Amended) A semiconductor integrated circuit device comprising:

a high-threshold N-channel type MIS field effect transistor, connected between a first real power supply line and a first pseudo power supply line;

a load circuit having a low-threshold MIS field effect transistor of a first conductivity type and a low-threshold MIS field effect transistor of a second conductivity type;

a level conversion circuit which receives a control signal of a first level for controlling said high-threshold N-channel type MIS field effect transistor, and which converts said control signal of said first level into a control signal of a second level and supplies said control signal of said second level to a gate of said high-threshold N-channel type MIS field effect transistor; and

a waveshaping circuit which receives the output signal of said level conversion circuit, and performs waveshaping so that an output signal of said waveshaping circuit rises slower than said control signal, wherein:

a first power supply terminal of said load circuit is connected to said first pseudo power supply line, and a second power supply terminal of said load circuit is connected to a second real power supply line; ~~and~~

an output signal of said waveshaping circuit is supplied to the gate of said high-threshold N-channel type MIS field effect transistor; and

said waveshaping circuit comprises a high-threshold final-stage MIS field effect transistor or a plurality of high-threshold final-stage MIS field effect transistors connected in series.

10. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 9, wherein said high-threshold N-channel type MIS field effect transistor ~~of said first conductivity type~~ and said level conversion circuit are together constructed as a module.

11. (Original) The semiconductor integrated circuit device as claimed in claim 9, wherein said first level is equal to a signal interface level of said load circuit, and said second level is a level greater than said first level.

12. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 9, wherein said first real power supply line is a real high-potential power supply line, said second real power supply line is a real low-potential power supply line, said first pseudo power supply line is a pseudo high-potential power supply

line, ~~and said high-threshold MIS field effect transistor of said first conductivity type is a high-threshold N-channel type MIS field effect transistor,~~ wherein:

a drain of said high-threshold N-channel type MIS field effect transistor is connected to said real high-potential power supply line, a source thereof is connected to said pseudo high-potential power supply line, and a back gate thereof is connected to said real low-potential power supply line.

13. (Currently Amended) A ~~The~~ semiconductor integrated circuit device ~~as claimed in claim 9~~ comprising:

a high-threshold P-channel type MIS field effect transistor, connected between a first real power supply line and a first pseudo power supply line;

a load circuit having a low-threshold MIS field effect transistor of a first conductivity type and a low-threshold MIS field effect transistor of a second conductivity type;

a level conversion circuit which receives a control signal of a first level for controlling said high-threshold P-channel type MIS field effect transistor, and which converts said control signal of said first level into a control signal of a second level and supplies said control signal of said second level to a gate of said high-threshold P-channel type MIS field effect transistor; and

a waveshaping circuit which receives the output signal of said level conversion circuit, and performs waveshaping so that an output signal of said waveshaping circuit rises slower than said control signal, wherein:

a first power supply terminal of said load circuit is connected to said first pseudo power supply line, and a second power supply terminal of said load circuit is connected to a second real power supply line;

an output signal of said waveshaping circuit is supplied to the gate of said high-threshold P-channel type MIS field effect transistor;

said first real power supply line is a real high-potential power supply line, said second real power supply line is a real low-potential power supply line, and said first pseudo power supply line is a pseudo high-potential power supply line[[,]]; and ~~said high-threshold MIS field effect transistor of said first conductivity type is a high-threshold P-channel type MIS field effect transistor, wherein:~~

a source and back gate of said high-threshold P-channel type MIS field effect transistor are connected to said real high-potential power supply line, and a drain thereof is connected to said pseudo high-potential power supply line.

14. (Cancelled)

15. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 9 [[14]], wherein said high-threshold N-channel type MIS field effect transistor ~~of said first conductivity type~~ is configured as a source follower, and a voltage on said first pseudo power supply line connected to the source of said high-threshold MIS field effect transistor of said first conductivity type rises in response to the rising output signal of said waveshaping circuit supplied to said gate.

16. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 9, wherein a physical shield is provided over a signal wiring line from said level conversion circuit to said high-threshold N-channel type MIS field effect transistor ~~of said first conductivity type~~.

17. (Original) The semiconductor integrated circuit device as claimed in claim 16, wherein said semiconductor integrated circuit device has a multilayered wiring structure, and said shield is formed in a prescribed intermediate wiring layer, while a signal line of a signal interface level of said load circuit is formed in a wiring layer located above said prescribed intermediate wiring layer.

18. (Cancelled)

19. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 9 [[14]], wherein said waveshaping circuit comprises a digital/analog converter.

20. (Original) The semiconductor integrated circuit device as claimed in claim 19, wherein said load circuit comprises a memory circuit, and said digital/analog converter outputs a voltage that is lower than a normal operating voltage of said memory and that only guarantees the retention of stored contents, thereby achieving a reduction in backup standby power consumption.

21-22. (Cancelled)

23. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 1, wherein said pseudo high-potential power supply line is brought outside a chip.

24. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 1, wherein said real high-potential power supply line is brought outside a chip.

25. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 8, wherein said pseudo high-potential power supply line is brought outside a chip.

26. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 8, wherein said real high-potential power supply line is brought outside a chip.

27. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 9, wherein said pseudo high-potential power supply line is brought outside a chip.

28. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 9, wherein said real high-potential power supply line is brought outside a chip.